ECDR-212-X
REFERENCE MANUAL

X = PCI, CPCI, PMC, PC104+

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1.0 OVERVIEW

1.1 Analog Data Input

The ECDR-212-X has two, transformer coupled, 50 Ω, inputs for input to the 12-bit A/D's (AD6640). A full-scale input to the A/D is 2 VPP (+10 dBm) and the 1 dB Bandwidth is typically 50 KHz to 250 MHz.

1.2 A/D Clocks

The A/D Clock has the most stringent and critical timing requirements. The digitization of baseband or IF inputs typically requires a very stable clock source to minimize the "apparent phase noise" which arises from non-uniform sampling. For coherent systems, this clock is also typically required to be coherent with a system-internal "master oscillator" so that the sampling is consistent with regard to other system variables.

The RMS jitter associated with commercially available chip-level Phase Locked Loops (PLL's) is typically unacceptable for A/D clock generation. Consequently, the ECDR-212-X is designed to accept an "External Clock Input" for generation of the A/D clock. The input circuitry for this clock consists of an AC-coupled differential PECL receiver that is stable in the absence of an active input. This input will generate a near perfect 50% duty cycle output from a sine wave input of +4 dBm to +10 dBm (1 VPP to 2 VPP into 50 ohms). When using a square wave input within this signal range, the output duty cycle will track that of the input.

1.3 Digital Receiver Clocks

In addition to the A/D a clock is required for the AD6620 Digital Receiver Chips. This clock may or may not be at the same rate as the A/D clock. This is due to the AD6620's provide for A/D input data "thinning" via the A/B Data Input Control and/or because the AD6620 FIR clock is permitted to be as high as 65 MHz, which may be an integer multiple of the input A/D data clock. The AD6620 FIR clock can be operated at 1, 2, or 4, times the rate of the A/D clock. It is generally desirable to operate this clock at the highest possible rate, since this permits the largest number of FIR taps to be used for a given application filter design. Also, it is generally desirable to operate the A/D at the highest possible clock rate since the receiver "processing gain" is achieved through the reduction of noise bandwidth via the filtering and associated data rate decimation process.

However, as the output data bandwidth requirement increases, the aliasing characteristics of the AD6620 second and fifth order CIC filters may present problems. In this event, it is usually best to "give up" 3 dB of processing gain (i.e., assuming the A/D is being clocked at one half the otherwise possible rate) by clocking in the A/D data at a rate below 32.5 MHz. Also it would be desirable to clock the AD6620 FIR clock at twice A/D clock (a factor of two is assumed, and typically all that is required). This is due to the fact that the AD6620 output data is clocked into the FIR section as I data followed by Q data and this is done at the FIR clock rate. Which, for a maximum of 65 MHz, requires a 32.5 MHz I and Q pair data rate (i.e., a 32.5 MHz maximum A/D input data rate, or the CIC2 filter must provide a decimation by at least two if the A/D input

data rate is 65 MHz). It should be noted that only the CIC2 filter can process the NCO I and Q pair output data at the full 65 MHz rate. Therefore, bypassing this filter and using the CIC5 filter to achieve a decimation by two is not possible since it has the same input data rate constraints as the FIR section. When the AD6620 A/D input data rate is less than the FIR clock rate (i.e., an integer sub-multiple of the FIR clock rate), this condition is detected by the ECDR-212-X hardware and the A/B Data Input Control is automatically handled for the user.

1.4 A/D and Receiver Clock Summary

The AD6620's require a Receiver Clock that determines the operating rate of the NCO, CIC2, CIC5, and FIR sections. This receiver clock must be 1, 2, or 4 times the A/D data input rate as selected in the clock control register. The maximum clock to the AD6620 is 65 MHz.

1.5 Channel/Receiver Configurations

There are 2 channels on the ECDR-212-X and each channel can use either 1 or 2 AD6620 Digital Receiver chips and each channel can select the A/D data from either of the two Analog Input Channels. A single AD6620 per channel provides sufficient processing capability for narrow bandwidth applications, while the use of dual AD6620's per channel provides equivalent performance for applications requiring up to twice the bandwidth. More specifically, the bandwidth, which can be supported by a single AD6620 is essentially determined by the number of taps required for adequate FIR filter performance.

By way of example, if a 64 tap FIR filter is adequate and the AD6620 is being clocked at 64 MHz, then the supported bandwidth can be up to 1 MHz. This is due to the minimum decimation permitted by the FIR section is equal to the number of taps (i.e., I and Q sample pairs will be output at a 1 MHz rate, supporting up to a 1 MHz analog bandwidth). The maximum number of taps supported by an AD6620 is 256, which would yield a maximum bandwidth per device of about 250 KHz at the maximum device clock rate of 65 MHz. For bandwidth requirements below this, the second-order and fifth-order CIC filters and FIR filter section can be combined with various decimation rates to further enhance receiver performance.

When two AD6620's are used for a single channel, they are operated the same but the FIR section of the second AD6620 is started after the first AD6620 FIR section has processed one half the number of taps. Thus, an I and Q sample pair will be output by the first AD6620 after the "number of taps" clocks, and one half the "number of taps" clocks later, an I and Q sample pair will be output by the second AD6620, and so on. It should be noted that an even number of taps (coefficients) must always be used in multi-AD6620 configurations to produce evenly spaced output samples (i.e., add a tap of value zero if necessary). Thus, the decimation is one half of what it would be for a single device, since it is now equal to one half the number of taps, and therefore can support twice the bandwidth.

The ECDR-212-X design takes this use of multiple AD6620's to obtain wider bandwidths one step further. The two channels can be combined to form a single channel with 4 AD6620's operating at one fourth the number of taps spacing to provide four times the bandwidth of a single device via decimation by one fourth the number of taps. This is programmable on a channel-pair basis and so a User could configure an ECDR-212-X to allow either AD to drive the AD6620's.

When channel-pairs are joined to form a single channel with twice the bandwidth capability, the FIFO's are "ping-ponged" as the outputs of the four AD6620's are written and must therefore be "ping-ponged" upon output to correctly order the I and Q sample pairs. This is handled automatically in the ECDR-212-X channel-pair control logic and is therefore transparent to the User. However, it should be noted that for this configuration, the FIFO depth is therefore twice that of a single channel.

1.6 Data Acquisition Modes

The ECDR-212-X has been designed to support both CW and pulsed system applications. Two basic data acquisition (operating) modes are made possible by an External Trigger, SMA connector, input which is provided on the front panel. The two basic modes are Sync and Gate with the Sync mode providing for a "counted burst" of data being collected, while the Gate mode provides an external control of the data processing interval, which can be anything up to and including continuous data processing (collection).

More specifically, the Sync mode treats the External Trigger Input like a synchronizing "trigger", the rising edge of which initiates the collection of a software programmed number of receiver channel output I and Q sample pairs. The User should be aware that the programmable counter is 16 bits wide, permitting collection of up to 64K sample pairs, which is more than the depth of the FIFO's (i.e., the FIFO's are 16K deep for the 2-channel configuration and 32K deep for the 1-channel configuration). Based on the number of AD6620's being used per channel and the resultant decimation, the hardware automatically accounts for any internal delays. Since the delays are accounted for the first I and Q sample pair collected (written to FIFO) corresponds to the first valid output for receiver processing starting with the first A/D data input following that trigger Input rising edge. This is made possible by the fact that the AD6620 CIC and FIR sections are essentially cleared by the occurrence of the trigger input and then start calculating with that next A/D input sample. Optionally, the AD6620 NCO can also be reset by each trigger input to provide a zero start phase, or any other start phase provided the AD6620 phase offset register is programmed to that desired phase (rather than zero), in support of pulsed coherent systems.

There is also an "equivalent" to the hardware trigger control input provided via software. This is implemented as a register bit that can be set to start a collection sequence and cleared to end the sequence for the "Gate" mode. Similarly, setting this bit will start the collection of the programmed number of samples in the "Sync" mode. However, it should be noted that this bit must be cleared prior to being set again for a subsequent collection sequence to be initiated.

1.7 DMA Engines

Data can be moved from the on board FIFO to PCI space by either reading the ECDR-212-X as a target or by using the on board DMA engine. The DMA engine is located in the PLX9080 Bus controller. In order not to be redundant here the vendor can provide the user with copies of the PLX9080 manual to assist in use of the board.

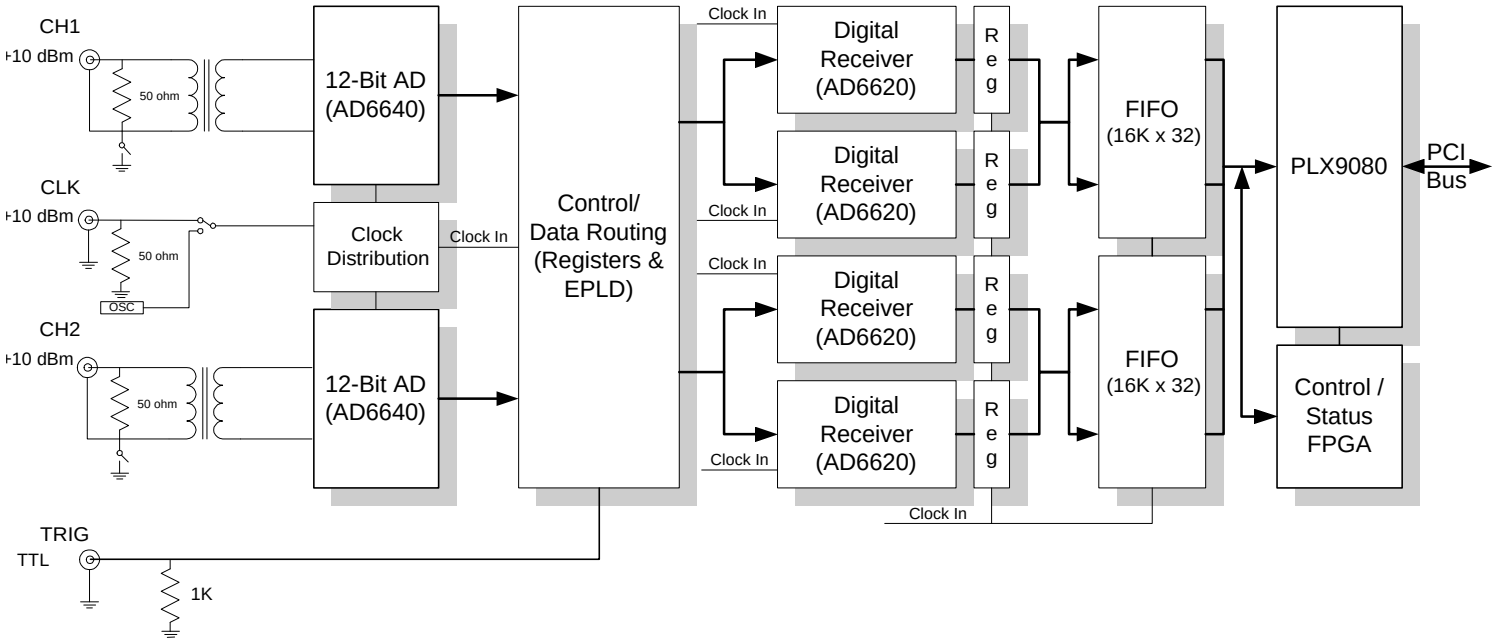

Figure 1
ECDR-212-X Block Diagram

2.0 SPECIFICATIONS

Physical Specifications				
Format	PC104+	PCI	CPCI	PMC
Size L x W	3.775 x 5.950	5.850 x 3.850	6.299 x 4.937	2.913 x 5.866
Power Supply Requirements Can be purchased with 5V only or with both 3.3 & 5V. Universal signally level	+5Vdc @ 2A +3.3Vdc @ TBD			
Connector Specifications				
Channel 1 Analog Input (J6)	Coax Type SMA P/N: 85SMA50-0-1			
Channel 2 Analog Input (J7)	Coax Type SMA P/N: 85SMA50-0-1			
Clock Input (J4)	Coax Type SMA P/N: 85SMA50-0-1			
Trigger Input (J5)	Coax Type SMA P/N: 85SMA50-0-1			

ENVIRONMENTAL SPECIFICATIONS

PARAMETER	OPERATING	STORAGE
Temperature	0- 70 ° C	-55 °C - + 100 °C
Relative Humidity	95% Non-Condensing	95% Non-Condensing
Cooling Requirement	A Linear Air Flow of > 2.5 Meters/sec is Recommended	N/A
Thermal Shock	! 5 °C/MIN	!10 ° C/Min
Altitude	-1000 – 10000 Feet	-1000 – 50000 Feet
Vibration	10 to 100 HZ @ 2G	10 to 500 HZ @ 2G
Mech Shock	20G for 6 MS (Half Sine) when mounted in a suitable racking system	
MTBF	> 100,000 Hours	N/A

3.0 REGISTER DESCRIPTION

3.1 ECDR-212-X Memory Map

The block memory map is shown in the table below. In order to access the memory on board the PLX9080 first needs to be configured for direct slave access. First the user must configure the PLX9080's PCI Command Register (PCICR) bits 1 &2. Once this is done the Local Address Space 0 Range and Local Base Address Registers (LAS0RR & LAS0BA) must be configured in the PLX9080.

Address Range Offset from Base address	**Description**
00 0000h to 00 FFFCh	ECDR-212-X Baseboard Register Space
01 0000h to 01 FFFCh	Receiver 1A Registers (see section 3.2 for details)
02 0000h to 02 FFFCh	Receiver 1B Registers (see section 3.2 for details)
03 0000h to 03 FFFCh	Receiver 2A Registers (see section 3.2 for details)
04 0000h to 04 FFFCh	Receiver 2B Registers (see section 3.2 for details)
05 0000h to 05 FFFCh	Digital Receiver #1 FIFO
06 0000h to 06 FFFCh	Digital Receiver #2 FIFO
07 0000h to 08 FFFCh	Digital Receiver #1 Gang Mode FIFO

3.2 ECDR-212-X Configuration Register Space

Address Offset	Abbreviation	Register Name	Attribute
0 0000h	CSR	Command/Status Register	Read/Write
0 0004h	RMODE	Receiver Mode Register	Read/Write
0 0008h	TCR	Trigger Command Register	Read/Write
0 000Ch	RDEC	Receiver Decimation Register	Read/Write
0 0010h	RBRST	Receiver Burst Count Register	Read/Write
0 0014-0 003Ch		* Reserved	Read/Write
0 0040h	INTCR	Interrupt Control Register	Read/Write
0 0044h	INTSR	** Interrupt Status Register	Read Only
0 0048h	FSTAT	** FIFO Status Register	Read Only
0 004Ch	CCR	Clock Control Register	Read/Write
0 0050h	RSTCMD	*** Reset Commands	Write Only
0 0054h	TIMER	Timer Register	Write Only
0 0058h	TEST	Test Register	Read Only
0 0044-0 FFFCh		* Reserved	

* Read/Writes will be acknowledged in order to allow burst access to register space.

** Read Only register however writes will be acknowledged in order to allow burst access to register space.

*** Write Only register however reads will be acknowledged in order to allow burst access to register space.

Register Name:	Command/Status Register
Abbreviation:	CSR
Address Offset:	0 000h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Receiver #1 Enable. Enables Receiver #1 data to be collected in Receiver #1 data FIFO during an acquisition: 0h=Disabled, 1h=Enabled.
																Receiver #2 Enable. Enables Receiver #2 data to be collected in Receiver #2 data FIFO during an acquisition: 0h=Disabled, 1h=Enabled.
																External Acquisition Gate Select. These bits select what external signal will be used for the Gate/Trigger input signal. This signal is always logically or'd with the software gate: 0h = Clock input Non-Inverted, 1h = Clock input Inverted.
																External Trigger Input Enable. This bit will enable the External Trigger Input. This bit has no affect on the software gate: 0h = Disabled 1h = Enabled.
																Acquisition Clock Configuration: 0h = Receiver clock greater than the acquisition clock, 1h = Receiver clock the same as the acquisition clock.
																Receiver Channels 1 Gate Active Status. This bit will be set to a one whenever a receiver channel is actively acquiring data: 0h = False, 1h = True.
																Receiver Channels 2 Gate Active Status. This bit will be set to a one whenever a receiver channel is actively acquiring data: 0h = False, 1h = True.
																Not Used

Register Name:	Receiver Mode Register
Abbreviation:	RMODE
Address Offset:	0 0004h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Receiver Channel 1 A/D Input Select. This will select the input signal source that receiver channel 1 will process. 0h = Analog A/D Channel 1, 1h = Analog A/D Channel 2.
																Receiver Channel 2 A/D Input Select. This will select the input signal source that receiver channel 2 will process. 0h = Analog A/D Channel 1, 1h = Analog A/D Channel 2.
																Receiver Channel 1 Dual Receiver Interleave Mode Enable (use 2 AD6620's and time interleave during data collection). 0h = Disabled, 1h = Enabled.
																Receiver Channel 2 Dual Receiver Interleave Mode Enable (use 2 AD6620's and time interleave during data collection). 0h = Disabled, 1h = Enabled.
																Receiver Channels 1 & 2 NCO Sync Enable. This bit is to enable Coherent Sampling - Starting the NCO at 0° Phase at the start of each Gate/Trigger. (CIC2, CIC5, and RCF Filters are always synchronized to the beginning of an acquisition). 0h = Disabled, 1h = Enabled.
																Receiver Channels 1 & 2 Counted Burst Mode Enable. This bit enables the gate/trigger input to be used as a trigger to collect the number of samples programmed in the Receiver Burst Count Register (RBRST). **Both receivers must be enabled in order to perform a counted burst.** 0h = Disabled (Gate Mode), 1h = Enabled (Counted Burst Mode)
																Quad Receiver Interleave Mode Enable. (use 4 AD6620's and time interleave them during data collection). This uses channels 1 and 2, and dual mode for channels 1 & 2 must also be enabled: 0h = Disabled, 1h = Enabled.
																Not Used

Register Name:	Trigger Command Register
Abbreviation:	TCR
Address Offset:	0 0008h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Gate/Trigger Command. This bit will act as any other source for the gate/trigger, except that it can not be disabled. When in gate mode this bit can provide a gate signal to the receivers. When in counted burst mode, this bit can provide a trigger. Note that the trigger is edge triggered, thus to re-trigger the trigger this bit must be cleared and set. When in Gate Mode: 0h=software gate is off, 1h=software gate is on. When in Counted Burst Mode: 0h=trigger is cleared, 1h=trigger is set.
																Not Used

Register Name:	Receiver Decimation Register
Abbreviation:	RDEC
Address Offset:	0 000Ch
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Total Decimation for Receiver Channel 1. The programmed value should equal one-half the Total Decimation of the AD6620 minus 1. This register must always be programmed to the correct value for the receiver channel to operate correctly. $\text{Value} = \frac{\text{Total Decimation}}{2} - 1$
																Not Used
																Total Decimation for Receiver Channel 2. The programmed value should equal one-half the Total Decimation of the AD6620 minus 1. This register must always be programmed to the correct value for the receiver channel to operate correctly. $\text{Value} = \frac{\text{Total Decimation}}{2} - 1$
																Not Used

Register Name:	Receiver Burst Count Register
Abbreviation:	RBRST
Address Offset:	0 0010h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Burst Count Value for Receiver Channels 1 and 2. This is the acquisition sample count – the number of samples that will be acquired when a trigger is received, and the burst counter is enabled in the Receiver Mode Register (RMODE): 0000h = Acquire 1 sample, 0001h = Acquire 2 samples, 3FFFh = Acquire 16384 samples.
																Not Used

Register Name:	Interrupt Control Register
Abbreviation:	INTCR
Address Offset:	0 0040h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Timer Interrupt Enable. This bit will enable a PCI interrupt to be set whenever the Timer has finished timing the programmed time interval in the (finished counting the specified number of clocks from the 33MHz clock). 0h = Disabled, 1h = Enabled.
																Start of Acquisition (Gate Start) Interrupt Enable. This bit will enable a PCI interrupt to be set whenever the acquisition gate becomes active. This interrupt is edge triggered, and must go from the inactive state to the active state to generate an interrupt: 0h = Disabled, 1h = Enabled.
																Gate Complete Interrupt Enable. This bit will enable a PCI interrupt to be set whenever the acquisition gate is returned to the inactive state or when a counted burst is complete. The first gate to complete from any of the receiver channels will trigger this interrupt: 0h = Disabled, 1h = Enabled.
																Receiver Channels 1 FIFO Half Full Interrupt Enable. This bit will enable the first receiver FIFO to become half full to generate a PCI interrupt. This is edge triggered: 0h = Disabled, 1h = Enabled.
																Receiver Channels 1 FIFO Full Interrupt Enable. This bit will enable the first receiver FIFO to become full to generate a PCI interrupt: 0h = Disabled, 1h = Enabled.
																Receiver Channels 2 FIFO Half Full Interrupt Enable. This bit will enable the first receiver FIFO to become half full to generate a PCI interrupt. This is edge triggered: 0h = Disabled, 1h = Enabled.
																Receiver Channels 2 FIFO Full Interrupt Enable. This bit will enable the first receiver FIFO to become full to generate a PCI interrupt: 0h = Disabled, 1h = Enabled.
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

Register Name:	Interrupt Status Register **(Reading this register will clear the local interrupt)**
Abbreviation:	INTSR
Address Offset:	0 0044h
Attribute:	Read Only

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Timer Interrupt Status. This bit reports the timer interrupt status. This is a local interrupt: 0h = False, 1h = True.
																Start of Acquisition (Gate Start) Interrupt Status. This bit reports the status of the start-of-acquisition. This is a local interrupt: 0h = False, 1h = True.
																Gate Complete Interrupt Status. This bit reports the status of the acquisition gate complete. The interrupt will also be generated when the counted burst is complete. This is a local interrupt: 0h = False, 1h = True.
																Receiver Channels 1 FIFO Half Full Interrupt Status. This bit reports the status of the Half full interrupt. This is a local interrupt: 0h = False, 1h = True.
																Receiver Channels 1 FIFO Full Interrupt Status. This bit reports the status of the full interrupt. This is a local interrupt: 0h = False, 1h = True.
																Receiver Channels 2 FIFO Half Full Interrupt Status. This bit reports the status of the Half full interrupt. This is a local interrupt: 0h = False, 1h = True.
																Receiver Channels 2 FIFO Full Interrupt Status. This bit reports the status of the full interrupt. This is a local interrupt: 0h = False, 1h = True.
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

Register Name:	FIFO Status Register
Abbreviation:	FSTAT
Address Offset:	0 0048h
Attribute:	Read Only

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Receiver #1 FIFO Status. These bits report the FIFO current status: 0h = FIFO Empty, 1h = FIFO has at least one, but <8K samples, , 3h = FIFO has >8K Samples, but <16K samples, 7h = FIFO has >16257 samples, Fh = FIFO is Full.
																Receiver #1 FIFO Status. These bits report the FIFO current status: 0h = FIFO Empty, 1h = FIFO has at least one, but <8K samples, , 3h = FIFO has >8K Samples, but <16K samples, 7h = FIFO has >16257 samples, Fh = FIFO is Full.
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

Register Name:	Clock Control Register
Abbreviation:	CCR
Address Offset:	0 004C
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Receiver Clock Frequency Range Select. These bits select what range the receiver clock will operate. 0h = Receiver clock is between 40MHz and 65MHz, 1h = Receiver clock is between 25MHz and 60MHz, 2h = Receiver clock is between 15 and 35MHz
																Receiver Clock Multiply Select. These bits select the multiply factor for the receiver clock: 0h=Multiply by 1, 1h=Multiply by 2, 2h=Multiply by 4.
																Not Used

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

Register Name:	Reset Commands
Abbreviation:	RSTCMD
Address Offset:	0 0050
Attribute:	Write Only

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Card Reset Command. Resets all logic and registers on the ECDR-212-X except PLX9080 registers: 0h = False, 1h = True.
																Receiver #1 FIFO Reset. Resets the Receiver Channel 1 Sample FIFO: 0h = False, 1h = True.
																Receiver #2 FIFO Reset. Resets the Receiver Channel 2 Sample FIFO: 0h = False, 1h = True.
																Receiver Channel 1 Reset. Resets the AD6620 Receivers for Channel 1: 0h = False, 1h = True.
																Receiver Channel 2 Reset. Resets the AD6620 Receivers for Channel 2: 0h = False, 1h = True.
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

Register Name:	Timer Register
Abbreviation:	TIMER
Address Offset:	0 0054
Attribute:	Write Only

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																32-bit value that is loaded into a counter that will generate and interrupt when the counter counts to 1. The counter runs off the 33 MHz system clock.
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																32-bit value that is loaded into a counter that will generate and interrupt when the counter counts to 1. The counter runs off the 33 MHz system clock.

Register Name:	Test Register
Abbreviation:	TEST
Address Offset:	0 0058
Attribute:	Read Only

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1	Read only register used verify operation
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
1	1	1	1	1	1	1	0	1	1	1	0	1	1	0	1	Read only register used verify operation

3.2 ECDR-212-X Receiver 1 through 2 Register Spaces

The ECDR-212-X Receiver 1 through 2 Register spaces are the same for each Channel. Each Receiver has two (2) AD6620 Receiver IC's, which need to be programmed (A or B). Each space is broken into 8 blocks, 4 for each receiver IC. When Receiver #X is to be programmed, the X is replaced by 1A, 1B, 2A, or 2B. **The Receiver Acquisition Clock must be connected before the receiver's can be programmed.**

The ECDR-212-X receiver memory map is shown in the table below.

Address Range Offset from Base address	**Description**
0000h – 03FCh	Receiver #X RAM Coefficient Filter (RCF) Coefficient RAM
0400h – 07FCh	Receiver #X RAM Coefficient Filter (RCF) Data RAM
0800h – 0BFCh	Receiver #X Reserved
0C00h – 0FFFh	Receiver #X Control Register Space

3.2.1 RCF Coefficient RAM

Memory which stores user-programmable coefficients for the RCF filter. The RAM will hold 256 20-bit twos complement words for a maximum filter length of 256 taps. In Dual Channel Real Mode, the filter length is limited to 128 taps per channel. The number of taps used is controlled by N_{TAPS} regardless of the number coefficient locations programmed.

3.2.2 RCF Data RAM

These locations store I and Q data exiting the CIC5 filter stage while the RCF performs multiply accumulates. The lower 18 bits of the 36-bit location is I data; the upper 18 bits are Q data. These locations are addressed in memory map and are available via the control ports so that the data RAM can be flushed for testing and simulation purposes. They are not cleared on reset as this would have added additional hardware; there are 256 36-bit locations.

3.2.3 ECDR-212-X Receiver #XX Control Register Space

The Receiver Control Register Space is the same for each Receiver's AD6620 Receiver IC.

The X in the 'Abbreviation', and in the 'Register Name' should be replaced by the receiver number desired. The Y in the 'Abbreviation', and in the 'Register Name' should be replaced by the receiver's AD6620 desired, A or B.

Address Offset	Abbreviation	Register Name	Attribute
0C00h	RxyMCR	Receiver #xy: Mode Control Register	Read/Write
0C04h	RxyNCOC	Receiver #xy: NCO Control Register	Read/Write
0C08h	RxyNCOS	Receiver #xy: NCO Sync Control Register	Read/Write
0C0Ch	RxyNCOF	Receiver #xy: NCO FREQ	Read/Write
0C10h	RxyNCOP	Receiver #xy: NCO Phase Offset	Read/Write
0C14h	RxyCIC2S	Receiver #xy: Input / CIC2 Scale Register	Read/Write
0C18h	RxyCIC2M	Receiver #xy: M_{CIC2} - 1	Read/Write
0C1Ch	RxyCIC5S	Receiver #xy: S_{CIC5}	Read/Write
0C20h	RxyCIC5M	Receiver #xy: M_{CIC5} - 1	Read/Write
0C24h	RxyRCFC	Receiver #xy: Output/RCF Control Register	Read/Write
0C28h	RxyRCFM	Receiver #xy: M_{RCF} - 1	Read/Write
0C2Ch	RxyRCFA	Receiver #xy: RCF Address Offset Register	Read/Write
0C30h	RxyRCFN	Receiver #xy: N_{TAPS} - 1	Read/Write
0C34h		Receiver #xy: Reserved (Should be written 00h)	Read/Write

Register Name:	Mode Control Register
Abbreviation:	RxyMCR
Address Offset:	0C00h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Soft_Reset
																Dual Channel Real Input Mode
																Single Channel Complex Input Mode
																Sync Master/Slave (Master=1, Slave=0)
																Reserved
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

This location brings the chip out of reset and sets the operating mode. It also specifies how the chip will use it's SYNC pins: as outputs while acting as a sync master or as inputs while acting as a sync slave. This is the only register with a defined power-up state: on power up, each bit will be at a logic "1". This places the chip in Soft_Reset and defines the chip as a sync slave. Powering up to a sync slave avoids contention problems when connecting multiple AD6620's.

If bit 0 is written low and bits 2 & 1 are low, then the AD6620 is in Single Channel Real Mode. If bit 1 is high and bits 0 & 2 are low, then the device is in the Dual Channel Real Mode. If bit 2 is high and bit 0 & 1 are low, then the chip is in the Single Setting bit 3 high configures the AD6620 as a SYNC master; SYNC pins are then used as outputs. If bit 3 is low the it is a SYNC slave, and the SYNC pins function as inputs. Bits 7-4 are reserved and should be written low.

Register Name:	NCO Control Register
Abbreviation:	RxyNCOC
Address Offset:	0C04h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																NCO Bypass (ByPass = 1, Active = 0)
																Enable Phase Dither
																Enable Amplitude Dither
																Reserved
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

This register allows control of some special features of the NCO. If bit 0 of this register is high, the NCO of the AD6620 is bypassed. When this is the base, both the I and Q data that are passed through the chip will be the same and the Spectrum will not be translated.

The NCO has two features to improve the performance of some systems: Phase Dither and Amplitude Dither. These can be used together or alone. If bit 1 of the register is high, then phase dither is activated. If bit 1 is low, then there is no phase dither in the NCO. If bit 2 is high, then the Amplitude Dither is activated, and if bit 2 is low, it is deactivated.

Register Name:	NCO Sync Control Register
Abbreviation:	RxyNCOS
Address Offset:	0C08h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Sync Mask LSW
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Sync Mask MSW

This holds the SYNC_MASK, which controls the frequency of the SYNC_NCO pulses and therefore the phase accuracy of the synchronization.

Register Name:	NCO FREQ
Abbreviation:	RxyNCOF
Address Offset:	0C0Ch
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																NCO Frequency LSW
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																NCO Frequency MSW

This register holds the NCO frequency control word. This is a 32 bit unsigned integer that sets the frequency of the AD6620 NCO.

Register Name:	NCO Phase Offset
Abbreviation:	RxyNCOP
Address Offset:	0C10h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																NCO Phase Offset LSW
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																NCO Phase Offset MSW

This register controls the phase offset of NCO. This can be used to allow for phase differences between multiple antennas receiving the same carrier.

Register Name:	Input / CIC2 Scale Register
Abbreviation:	RxyCIC2S
Address Offset:	0C14h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																S_{CIC2}
																Reserved
																ExpInv
																ExpOff
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

This register holds the scale factor, S_{CIC2}, for CIC2. S_{CIC2} scales down the data before it is accumulated in CIC2. This avoids register wrap-around in the twos-complement arithmetic and eliminates the resulting spectral errors. S_{CIC2} is contained in bits 2-0 of this register. It is treated as an unsigned integer between 0 and 6. Increasing S_{CIC2} shifts data down.

The second function of this register is to scale the input data from the Parallel Data Input port. This allows the AD6620 to treat the floating point input data with considerable flexibility. There are two parts of this function. The first is bit 4 which tells the AD6620 how to handle the exponent, EXP[2:0]. If this bit is low, then data is shifted down as the exponent increases. If this bit is high, then for increasing EXP[2:0] the input data is shifted up. The second part of the input data shifting is the Exponent Offset (ExpOff[7..5]) held in bits 7-5 of this register. This provides gain to the input.

Register Name:	M_{CIC2} - 1
Abbreviation:	RxyCIC2M
Address Offset:	0C18h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																CIC2 Decimation Minus One
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

This register controls the amount of decimation in the CIC2 filter stage. The value contained in this register is the CIC2 decimation rate minus one. This is interpreted as an unsigned 8-bit integer but due to limited growth in the CIC2 filter accumulators, this value should normally be limited to 15 (decimation =16).

Register Name:	S_{CIC5}
Abbreviation:	RxyCIC5S
Address Offset:	0C1Ch
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																S_{CIC5}
																Reserved
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

This register holds the scale factor for CIC5. This is used to scale down the data before it is accumulated in CIC5. This avoids register wrap-around in the twos-complement arithmetic and eliminates the resulting spectral errors. The value is contained in bits 4-0 of this register. It is treated as an unsigned integer between 0 and 20. Increasing this value shifts data down.

Register Name:	M_{CIC5} - 1
Abbreviation:	RxyCIC5M
Address Offset:	0C20h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																CIC5 Decimation Minus One
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

This register controls the amount of decimation in the CIC5 filter stage. The value contained in this register is the CIC5 decimation rate minus one. This is interpreted as an unsigned 8-bit integer but due to limited growth in the CIC5 filter accumulators, this value should normally be limited to 31 (decimation = 32).

Register Name:	Output/RCF Control Register
Abbreviation:	RxyRCFC
Address Offset:	0C24h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Output Scale Factor
																Reserved
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

Bits 2-0 of this register hold the Output Scale Factor, S_{OUT}. These bits are interpreted as a 3-bit unsigned integer, the value of which controls which of the 23 output bits of the RCF are passed to the output port being used. The data Output corresponds to the following equation where OL_{RCF} is the 23-bit output of the RCF and POL is the 16-bit data available at the parallel output port or the serial port when 16-bit serial words are used. The truncation function rounds the scaled 23-bit number to 16 bits.

$$POL = round(OL_{RCF} \text{ A } 2^{(SOUT-1)},16)$$

Bits 7-3 of this register are reserved and must be written 0.

Register Name:	M_{RCF} - 1
Abbreviation:	RxyRCFM
Address Offset:	0C28h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																RCF Decimation Minus One
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

This register controls the amount of decimation in the RCF filter stage. The value contained in this register is the RCF decimation rate minus one. This is interpreted as an unsigned 8-bit integer, but due to limited number of taps and, therefore, filtering power in the RCF filter accumulators this value should be limited to 31 (decimation = 32).

Register Name:	RCF Address Offset Register
Abbreviation:	RxyRCFA
Address Offset:	0C2Ch
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Filter Coefficient Address Offset
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

This register controls the address offset used by the RCF to calculate a given filter and is interrupted as an 8-bit unsigned integer. It allows more the one filter to be placed in the Coefficient RAM. This makes it possible to switch filters without reloading all of the coefficients. The RCF filter will compute taps for all coefficients between RCF_{OFF} and (RCF_{OFF} + N_{TAPS}) provided the decimation, clock rate and input data rate provide sufficient time for this.

Register Name:	N_{TAPS} - 1
Abbreviation:	RxyRCFN
Address Offset:	0C30h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Number of Taps Minus One
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

This register controls the number of taps calculated by the RCF. The value in this register is interpreted as an unsigned integer and is equal to the number of taps desired minus one. This filter is not inherently symmetric and the number coefficients place in the Coefficient RAM will be equal to the number of taps, provided that only one filter at a time is loaded. No symmetry is assumed and preaddition is not used. The total number of taps for all filters must be less than 256 taps for Single Channel Real Mode, or less than 128 taps/channel for Diversity Channel Real Mode.

Register Name:	M_{RCF} - 1
Abbreviation:	RxyRCFM
Address Offset:	0C28h RxyRCFA
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																RCF Decimation Minus One
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

This register controls the amount of decimation in the RCF filter stage. The value contained in this register is the RCF decimation rate minus one. This is interpreted as an unsigned 8-bit integer but due to limited growth in the RCF filter accumulators, this value should be limited to 32.

Register Name:	RCF Address Offset Register
Abbreviation:	RxyRCFA
Address Offset:	0C2Ch
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Filter Coefficient Address Offset
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

This register controls the address offset used by the RCF to calculate a given filter and is interpreted as an 8-bit unsigned integer. It allows more than one filter to be placed in the Coefficient RAM. This makes it possible to switch filters without reloading all the coefficients. The RCF filter will compute taps for all coefficients between RCF_{OUT} and (RCF_{OUT} + N_{TAPS}) provided that the decimation, CLK rate and input data rate provide sufficient time for this.

Register Name:	N_{TAPS} - 1
Abbreviation:	RxyRCFN
Address Offset:	0C30h
Attribute:	Read/Write

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Number of Taps Minus One
																Not Used
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

This register controls the number of taps calculated by the RCF. The value in this register is interpreted as an unsigned integer and is equal tot he value of the number of taps desired minus one. This filter is not inherently symmetric and the number of coefficients placed in the Coefficient Ram will be equal to the number of taps provided that only one filter is loaded at a time. No symmetry is assumed and pre-addition is not used.

4.0 TYPICAL APPLICATIONS

The ECDR-212-X has been designed as a "generic" multi-channel receiver for applications such as radar (pulsed and CW), Magnetic Resonance Imaging (MRI) (pulsed), and communications (CW). While detailed examples of numerous different applications is beyond the scope of this Applications Note, an overview of typical pulsed and CW applications is presented. In both cases, it is assumed that the user is supplying the A/D's clock and has already established the Receiver Clock rate, per the previously presented discussions. It is also assumed that the user has configured the AD6620's and loaded the FIR coefficients, consistent with the application requirements and previous discussions.

As a note/reminder to users involved with narrow pulse (and therefore wideband) applications such as high resolution tracking radar, there may be a constraint on the number of taps (coefficients) which can be used by the FIR filter without degrading the resolution of the radar. Typically, the constraint is that the number of taps times the tap spacing cannot exceed twice the pulse width. Thus, if the FIR is being clocked at 65 MHz (about 15.38 nanoseconds) and the transmitted pulse width is 400 nanoseconds, then the maximum number of taps which can be used is 52 (i.e., 800/15.38=52). Such applications will also typically interleave the AD6620's to minimize receiver decimation for a given number of taps in support of wider bandwidth requirements.

4.1 Typical Pulsed Application Usage

In general, pulsed applications involve a Pulse Repetition Frequency (PRF) which determines the rate at which data collection sequences must occur. A "trigger" pulse is normally available to indicate when the transmitter is starting to transmit a pulse and will therefore occur at the PRF. This "trigger" pulse is normally used as the ECDR-212-X "Trigger Input", either directly or indirectly, to establish the start time for receiver data collection (I and Q sample pairs being written to FIFO). An example of indirect usage would be to use the "trigger" pulse to produce a delayed output pulse, which in turn becomes the input Trigger signal. If such a delay is programmable, then the start of data collection can be varied in time, which for a radar, would correspond to a variable delay in range from the radar. Similarly, applications such as MRI may employ a fixed delay to provide a receiver "blanking" interval such that the receiver is essentially "disabled" during the time of pulse transmission. Thus, only true "return" data for that pulse would be processed.

If the radar is coherent, then the use of the "constant phase" (i.e., clear the NCO phase to zero or other fixed phase value) at the start of receiver data processing feature would be required. For a non-coherent MRI application, this feature would not be required. However, both applications would rely on the fact that at the activation of the trigger signal, the receiver processing chain is cleared. Following the clearing of the receiver processing chain the subsequent "first" output I and Q sample pair written to FIFO will result from processing which began with the first A/D data sample following that trigger signal activation. This is particularly important to applications like MRI where the transient response to a stimulus pulse is of interest. It is also important to radar applications because the exact "range" at which processing starts is well defined. In fact, if very accurate radar range determination is required, then the placement of the trigger activating edge relative to the A/D Clock (encode command) must also be tightly controlled by the user.

Given that the user now has control over where receiver data collection begins, it is now appropriate to determine where receiver data collection is to end. There are two modes (options) which are available: “Sync” mode, which collects a programmed number (up to 64K) of I and Q sample pairs, and “Gate” mode, which collects I and Q sample pairs for as long as the trigger signal is active. Applications that require a known, fixed number of samples, will typically use the “Sync” mode. An exception to this could be a radar application where, for a given transmitted waveform, the “range extent” for which data is to be collected varies at a rate sufficient to preclude re-programming the appropriate receiver channel-pair data collection counter. Such might be the case for a multiple-target tracking radar which varies the width of the “track gate” (data collection interval) as a function of track quality (i.e., degree of uncertainty as to actual target location) for each target.

4.2 Typical CW Application Usage

In general, CW applications involve receiver processing of the phase-modulated or frequency-modulated CW waveforms associated with radar or communications systems. For applications where there is an abrupt change (for example, a jump in frequency for radar range determination), the application may more closely resemble the above discussed pulsed systems and, as such, is not presented here. Rather, this discussion will address the more common “wireless” communications receiver applications requiring essentially “continuous” data throughput. These applications typically involve wideband, multi-channel wideband, and multi-channel narrowband receiver data processing requirements.

The ECDR-212-X provides two analog input channels which can be digitized by the resident AD6640 A/D’s. These A/Ds can be routed to the two AD6620’s which can be interleaved, a single channel can support bandwidths of up to 2 MHz. Interleaving channel pairs (i.e., using four AD6620’s to form a single channel) then supports bandwidths of up to 4 MHz.

The ECDR-212-X provides two analog input channels which can be digitized by the resident AD6640 A/D's. Thus, either diversity, or two independent analog IF inputs, may be processed by the receiver channels. This is further supported by the fact that each channel can be independently "tuned" as to down conversion frequency, thereby supporting both common and different frequency bands. For diversity applications, two A/D data channels would be used by two receiver channels, with these receiver channels tuned to the same frequency. Additional pairs of receiver channels would then support the simultaneous processing of multiple frequency bands. A similar situation would exist for two IF inputs, each associated with a different receiving antenna polarity (horizontal and vertical, for example).

5.0 BOARD MAINTENANCE

The ECDR-212-X design employs “programmable logic” in the form of EPLD’s and FPGA’s to maximize the flexibility with which the design can be modified to accommodate application requirements. These EPLD’s and FPGA’s are re-programmable on the board, but this should be done by returning the board to the vendor for upgrade and retest.

The significance of this re-programmability is that new “features” can be added, as the need arises, to provide additional application-specific functionality. Also, it should be noted that the ECDR-212-X is a rather complex product and, despite extensive testing at the vendor prior to “release”, it is anticipated that some user configurations may uncover “bugs” which had previously gone undetected. These bugs can be more easily alleviated owing to the re-programmable devices associated with those elements of the design where such problems are most likely to occur.

6.0 SWITCH DESCRIPTION

6.1 Module Slot Position (PC104+ Only - S1)

The only switch on the ECDR-212-X is the rotary switch that selects the module slot position as identified in the PC104+ specification. The effect of this switch is shown in the table below.

Switch Position	Module Slot	REQ*	GNT*	CLK	ID Address	INT0*
0 or 4	1	REQ0*	GNT0*	CLK0	AD20	INTA*
1 or 5	2	REQ1*	GNT1*	CLK1	AD21	INTB*
2 or 6	3	REQ2*	GNT2*	CLK2	AD22	INTC*
3 or 7	4	REQ2*	GNT2*	CLK3	AD23	INTD*

6.2 Data Order Switch

When position 1 of this switch is "ON", the data is read from the board with the I as the lower word and the Q as the upper word. This data order is reversed if position 1 is "OFF".

PC104+	N/A
PMC	S1
PCI	S1
CPCI	S1

6.3 Channel Input Isolation

This switch allows the user to isolate the channel from the ECDR-212-X ground or to connect the input return to this ground. If either position is in the "ON" position, then the return is connected to ground

Channel 1	S2
Channel 2	S3

6.4 Clock Selection (S4)

This switch allows the user to operate from an external clock or to use the on-board 65 MHz oscillator.

Pos 1	Pos 2	Clock
OFF	OFF	No Clock
ON	OFF	External
OFF	ON	Internal (65 MHz)
ON	ON	No Clock (Avoid)

7.0 INPUT CONNECTOR DESCRIPTION

Connector	Function
J6	Channel 1 Input
J7	Channel 2 Input
J4	External Clock Input
J5	External Trigger Input